

Figure 1

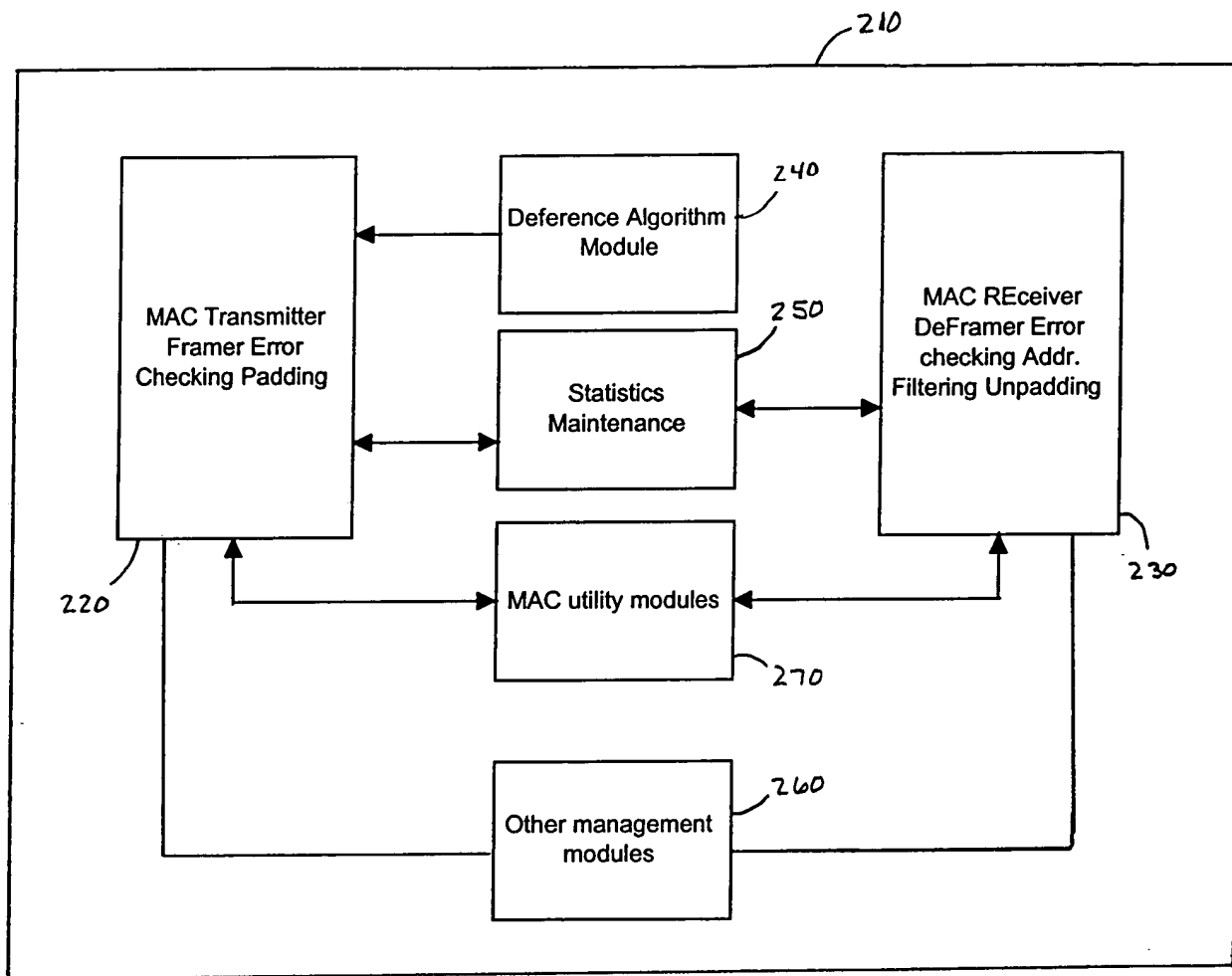


Figure 2

300

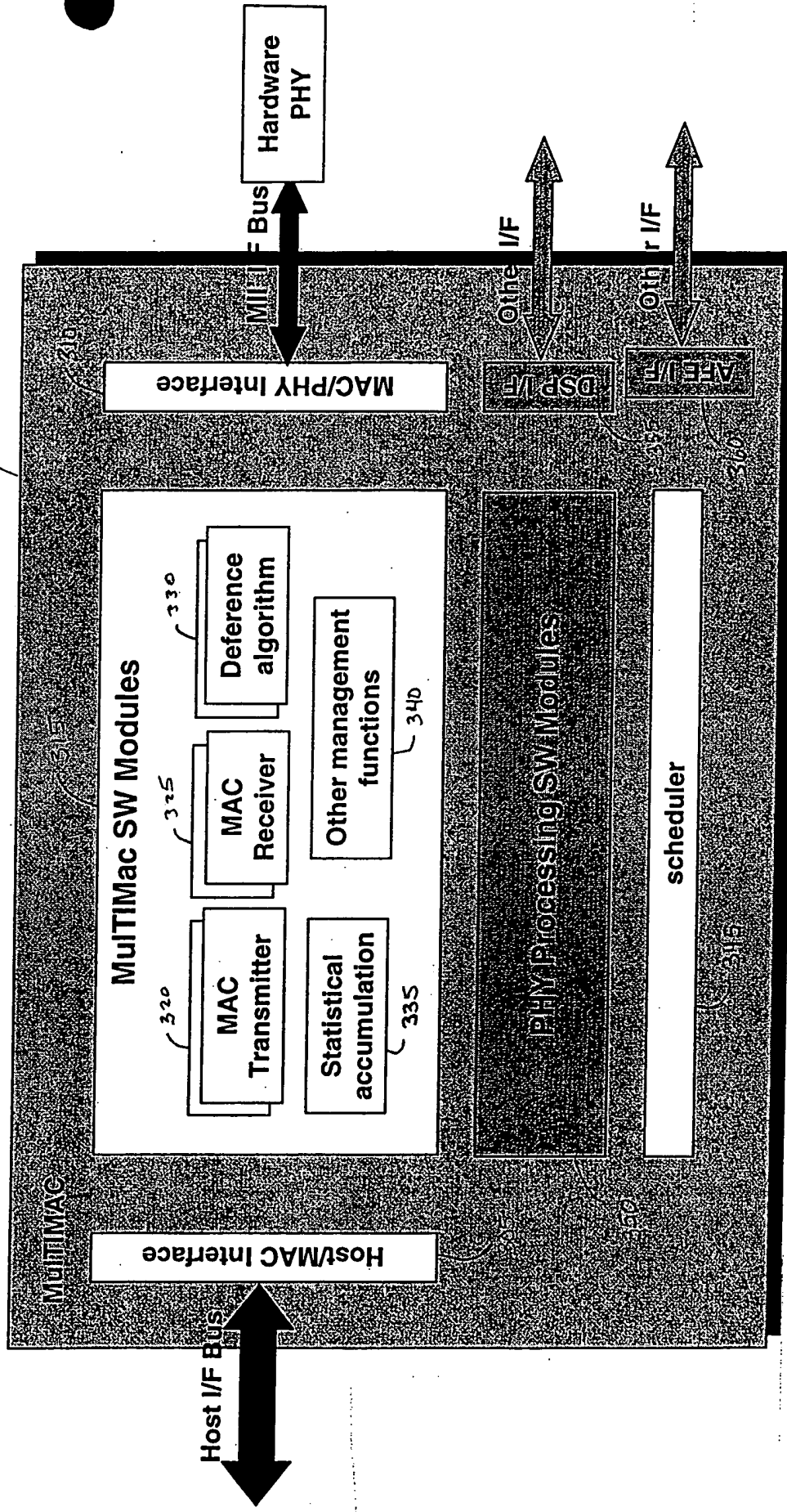


Figure 3

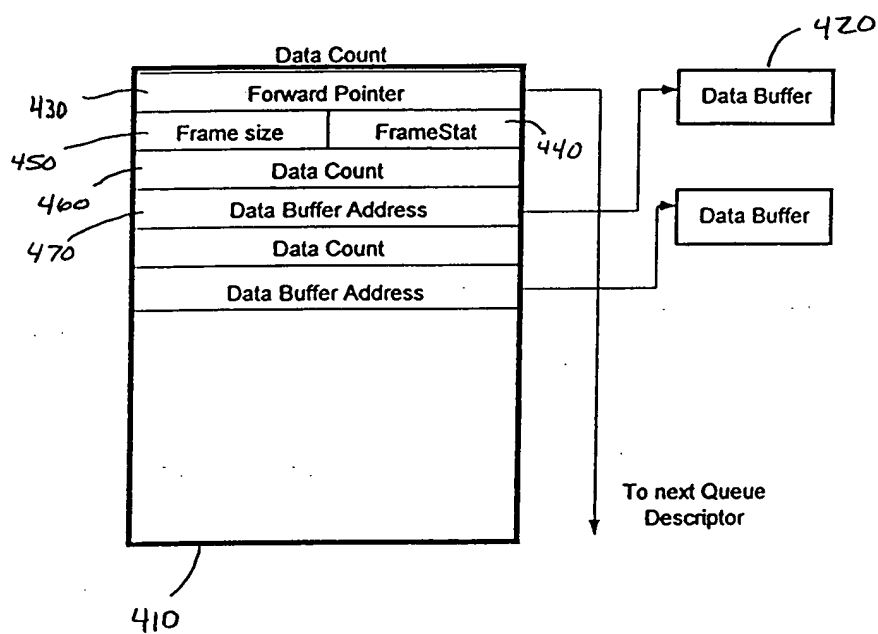


Figure 4

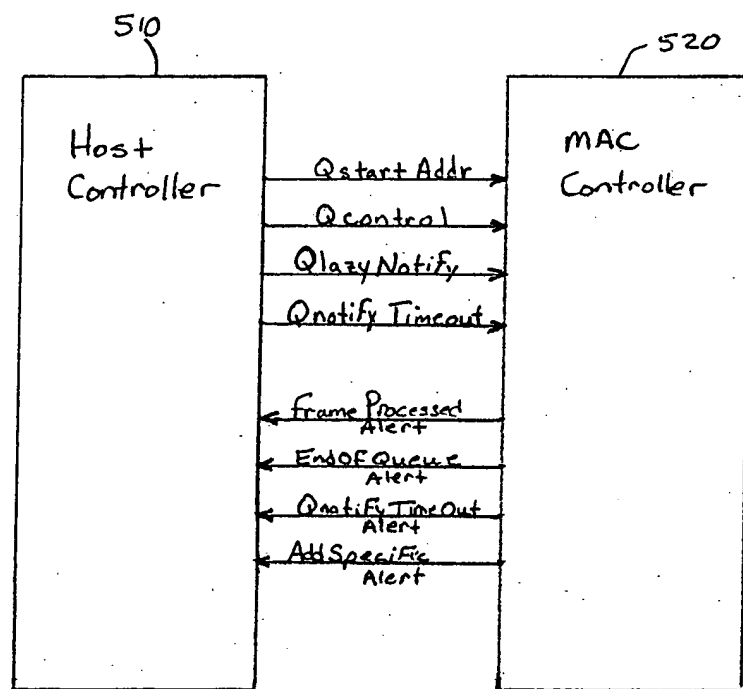


Figure 5

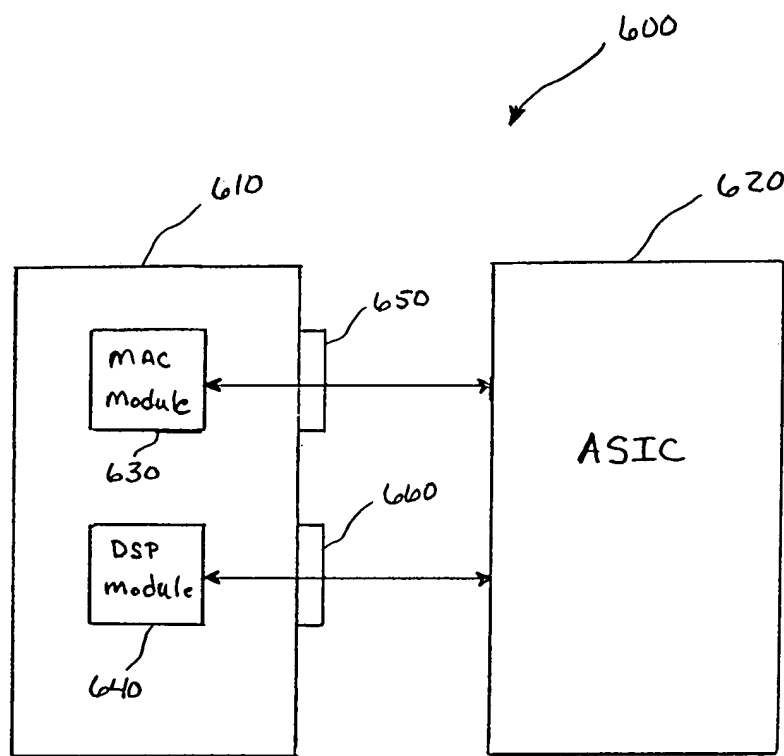


Figure 6

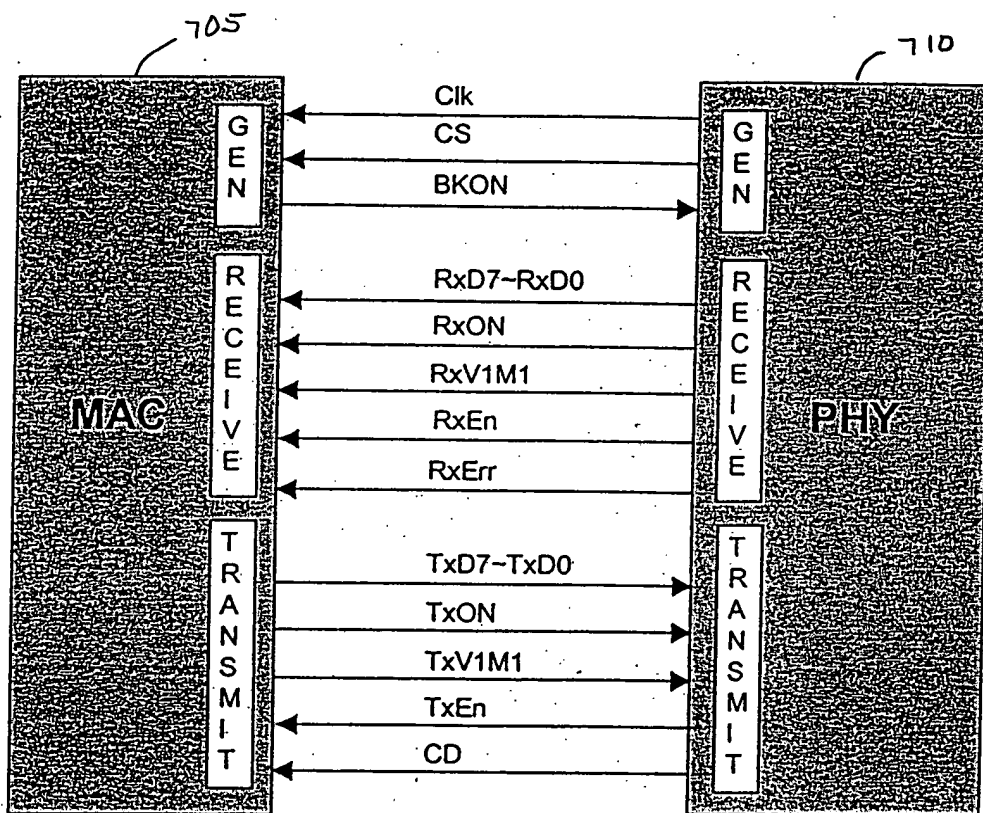


Figure 7

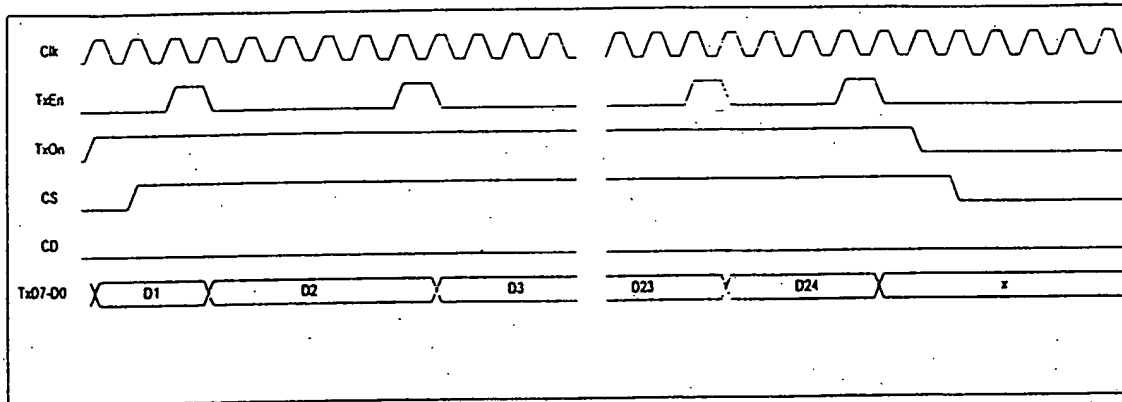


Figure 8

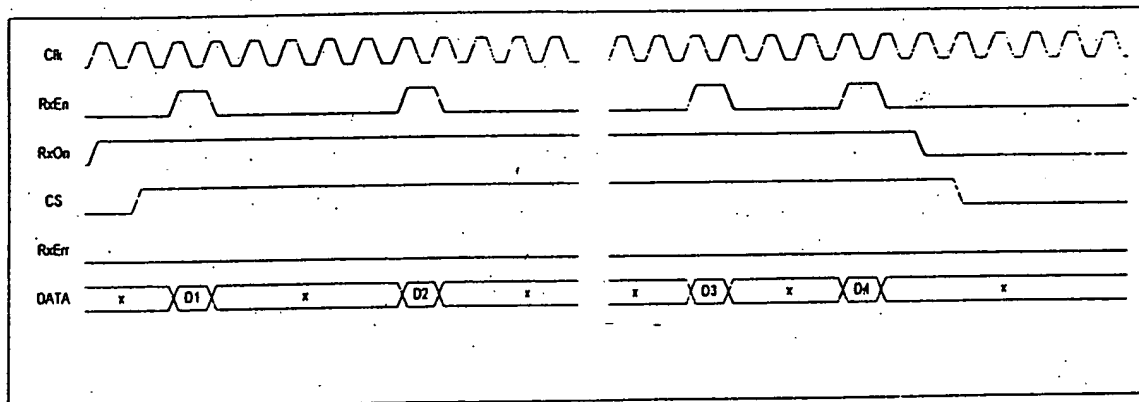


Figure 9

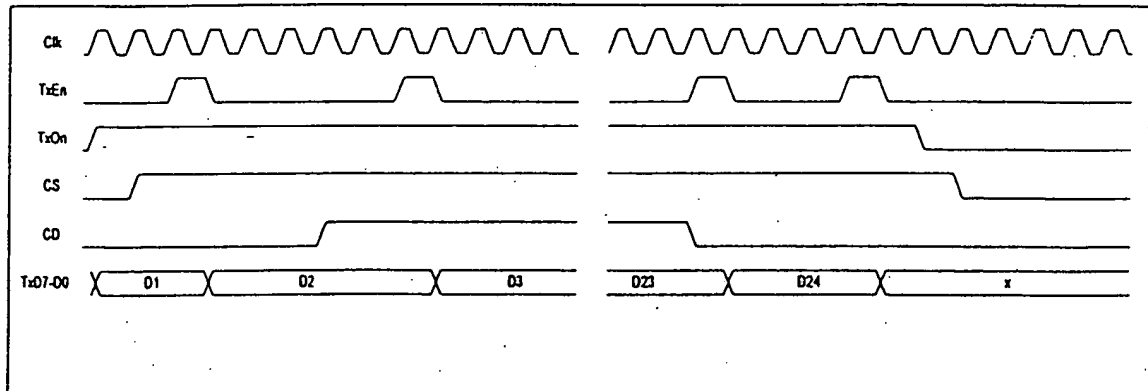


Figure 10

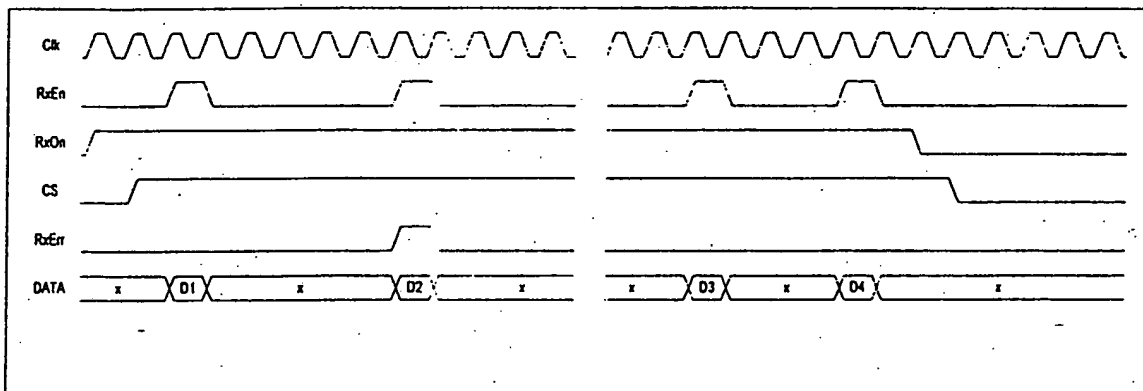


Figure 11

Register Address	Register Name	Description	R/W	Implementation
0	Tx address register	TxFrame start address	MAC write	MAC
1	Tx length register	TxFrame length	MAC write	PHY
2	Rx address register	RxFrame start address	MAC write	MAC
3	Rx length register	RxFrame length	MAC read	PHY
4	control register	frame transmit and receive control register	MAC write	MAC
5	status register	PHY signaling status	MAC read	MAC
6	interrupt mask register	PHY to MAC interrupt masks	MAC write	MAC
7	interrupt status register	Interrupt status	MAC read	MAC
8	CRC32 high register	CRC32 High 16 bits	MAC read	PHY
9	CRC32 low register	CRC32 Low 16 bits	MAC read	PHY
10	CRC16 register	CRC16	MAC read	PHY
11	PHY management control register	described in 5.	Host/MAC write	PHY
12	PHY management status register	described in 5.	Host/MAC read	PHY

Figure 12

Bits	Name	Description	R/W
15	TxON	1 = set TxON signal 0 = clear TxON signal	R/W
14	BkON	1 = set BkON signal 0 = clear BkON signal	R/W
13	TxVIM1	1 = set TxVIM1 signal 0 = clear TxVIM1 signal	R/W
12 ~ 8	Reserved	Write as 0, ignore on Read	R/W
7	Interrupt enable	1 = PHY Interrupts are globally enabled 0 = PHY interrupts are globally disabled	R/W
6 ~ 0	Reserved	Write as 0, ignore on Read	R/W

Figure 13

Bits	Name	Description	R/W
15	TxON	1 = TxON signal is asserted 0 = TxON signal is not asserted	R
14	BkON	1 = BkON signal is asserted 0 = BkON signal is not asserted	R
13	TxV1M1	1 = TxV1M1 signal is asserted 0 = TxV1M1 signal is not asserted	R
12	RxON	1 = RxON signal is asserted 0 = RxON signal is not asserted	R
11	CS	1 = CS signal is asserted 0 = CS signal is not asserted	R
10	CD	1 = CD signal is asserted 0 = CD signal is not asserted	R
9	RxV1M1	1 = RxV1M1 signal is asserted 0 = RxV1M1 signal is not asserted	R
8	RxErr	1 = RxErr signal is asserted 0 = RxErr signal is not asserted	R
7	Interrupt enable	1 = PHY interrupts are globally enabled 0 = PHY interrupts are globally disabled	R
6 ~ 0	Reserved	ignore on Read	R

Figure 14

Bits	Name	Description	R/W
15	CS_ON enable	1 = enable interrupt when CS signal becomes asserted 0 = disable CS_ON interrupt	R/W
14	CS_OFF enable	1 = enable interrupt when CS signal becomes de-asserted 0 = disable CS_OFF interrupt	R/W
13	CD_ON enable	1 = enable interrupt when CD signal becomes asserted 0 = disable CD_ON interrupt	R/W
12	RxON_ON enable	1 = enable interrupt when RxOn signal becomes asserted 0 = disable RxON+ON interrupt	R/W
11	RxON_BkON enable	1 = enable interrupt when RxOn signal becomes asserted during the backoff slots 0 = disable RxON_BkOn interrupt	
10	RxErr_ON enable	1 = enable interrupt when RxErr signal becomes asserted 0 = disable RxErr+ON signal	R/W
9	PHY RxFifo Overrun enable	1 = enable interrupt when PHY's receive fifo overrun 0 = disable the interrupt	R/W
8	PHY TxFifo Underrun Enable	1 = enable interrupt when PHY's transmit fifo is underrun 0 = disable the interrupt	R/W
7	PHY Sample Data Ready Enable	1 = enable interrupt when PHY's sample data is ready for DSP processing 0 = disable the interrupt	R/W
6	PHY Log Data Ready	1 = enable interrupt when PHY's log data is ready for DSP/Host to sample 0 = disable the interrupt	R/W
5~0	Reserved	Initialized with 0 and ignore on Read	R/W

Figure 15

Bits	Name	Description	R/W
15	CS_ON	1 = interrupt of CS signal becomes asserted has been generated 0 = CS_ON interrupt is not generated	R
14	CS_OFF	1 = interrupt of CS signal becomes asserted has been generated 0 = CS_OFF interrupt is not generated	R
13	CD_ON	1 = interrupt of CD signal becomes asserted has been generated 0 = CD_ON interrupt is not generated	R
12	RxON_ON	1 = interrupt of RxON_ON signal becomes asserted has been generated 0 = RxON_ON interrupt is not generated	R
11	RxOn_Bk ON	1 = interrupt of RxOn signal becomes asserted during the back off slots has been generated 0 = RxON_BkON interrupt is not generated	R
10	RxErr_ON	1 = an interrupt of RxErr signal becomes asserted has been generated 0 = RxErr ON interrupt is not generated	R
9	PHY RxFifo Overrun	1 = an interrupt of PHY's receive fifo overrun has been generated 0 = this interrupt is not generated	R
8	PHY TxFifo Underrun	1 = an interrupt of PHY's transmit fifo is underrun has been generated 0 = this interrupt is not generated	R
7	PHY Sample Data Ready	1 = an interrupt of PHY's sample data is ready for DSP processing has been generated 0 = this interrupt is not generated	R
6	PHY Log Data	1 = an interrupt of PHY's log data is ready for DSP/Host to sample 0 = this interrupt is not generated	R
5 ~ 0	Reserved	ignore on Read	R

Figure 16

Bits	Name	Description	R/W
15	Reset	1 = PHY reset	R/W
14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
13	Baudrate Selection	1 = 4Mbaud supported 0 = 4Mbaud not supported	R/W
12, 11	Mode selection	0 0 = 2.0 Mode 0 1 = 1.0 Mode 1 0 = Compatibility Mode 1 1 = Mode automatic selection	R/W
10	Collision Test	1 = enable CD signal test 0 = disable CD signal test	R/W
9	Power Mode	1 = Low power state 0 = normal power state	R/W
8:0	Reserved	Write as 0, ignore on Read	R/W

Figure 17

Bits	Name	Description	R/W
15	Reserved	Write as 0, ignore on Read	R
14	Loopback	1 = PHY is in loopback mode 0 = PHY is not in loopback mode	R
13	Baudrate Selection	1 = PHY supports 4Mbaud 0 = PHY does not support 4Mbaud	R
12, 11	Mode status	0 0 = PHY is in 2.0 only Mode 0 1 = PHY 1.0 only Mode 1 0 = PHY is in Compatibility Mode 1 1 = PHY is in automatic selection mode	R
10	Reserved	Write as 0 ignore on Read	R
9	Power Mode	1 = PHY is in Low power state 0 = PHY is in normal power state	R
8:0	Reserved	Write as 0, ignore on Read	R/W

Figure 18

Register Index	Register Name	Description	R/W	Implementation
0	TxFrame length	Byte count of frame transmitted from MAC to PHY	PHY read	PHY
1	RxFrame length	Byte count of frame transmitted from PHY to MAC	PHY write	PHY
2	Signal control	MAC/PHY interface signal control register	PHY write	PHY
3	Signal status	MAC/PHY signaling status	PHY read	PHY
4	CRC32 high register	CRC32 High 16 bits	PHY write	PHY
5	CRC32 low register	CRC32 Low 16 bits	PHY write	PHY
6	CRC16 register	CRC16	PHY write	PHY
7	PHY management control register	described in 5.0	PHY read	PHY
8	PHY management status register	described in 5.0	PHY write	PHY

Figure 19

Bits	Name	Description	R/W
15	RxON	1 = set RxON signal 0 = clear RxON signal	R/W
14	RxVIM1	1 = set RxVIM1 signal 0 = clear RxVIM1 signal	R/W
13	CS	1 = set CS signal 0 = clear RX signal	R/W
12	CD	1 = set CD signal 0 = clear CD signal	R/W
11	RxErr	1 = set RX signal 0 = clear RxErr signal	R/W
10 ~ 0	Reserved	Write as 0, ignore on Read	R/W

Figure 20

00000000000000000000000000000000

Register Index	Register Name	Description	R/W	Implementation
0	Sample data address	Sample data buffer start address	DSP write	DSP
1	Sample data length	The number of data bytes need to be transferred from the PHY	DSP write	DSP
2	Rx Sample data length	The number of data words (16 bit) actually transferred from the PHY	DSP read	PHY
3	DSP data length	The number of data words (16 bit) actually transferred from the PHY	DSP read	PHY
4	DSP data port	DSP data output port	DSP write	DSP

Figure 21

Register Index	Register Name	Description	R/W	Implementation
0	Rx Sample data length	The number of data words (16 bit) actually transferred from the PHY to the DSP	PHY write	PHY
1	DSP data length	The number of data bytes needed to be transferred to the PHY	PHY read	DSP
2	DSP data port	DSP data input port	PHY read	PHY

Figure 22

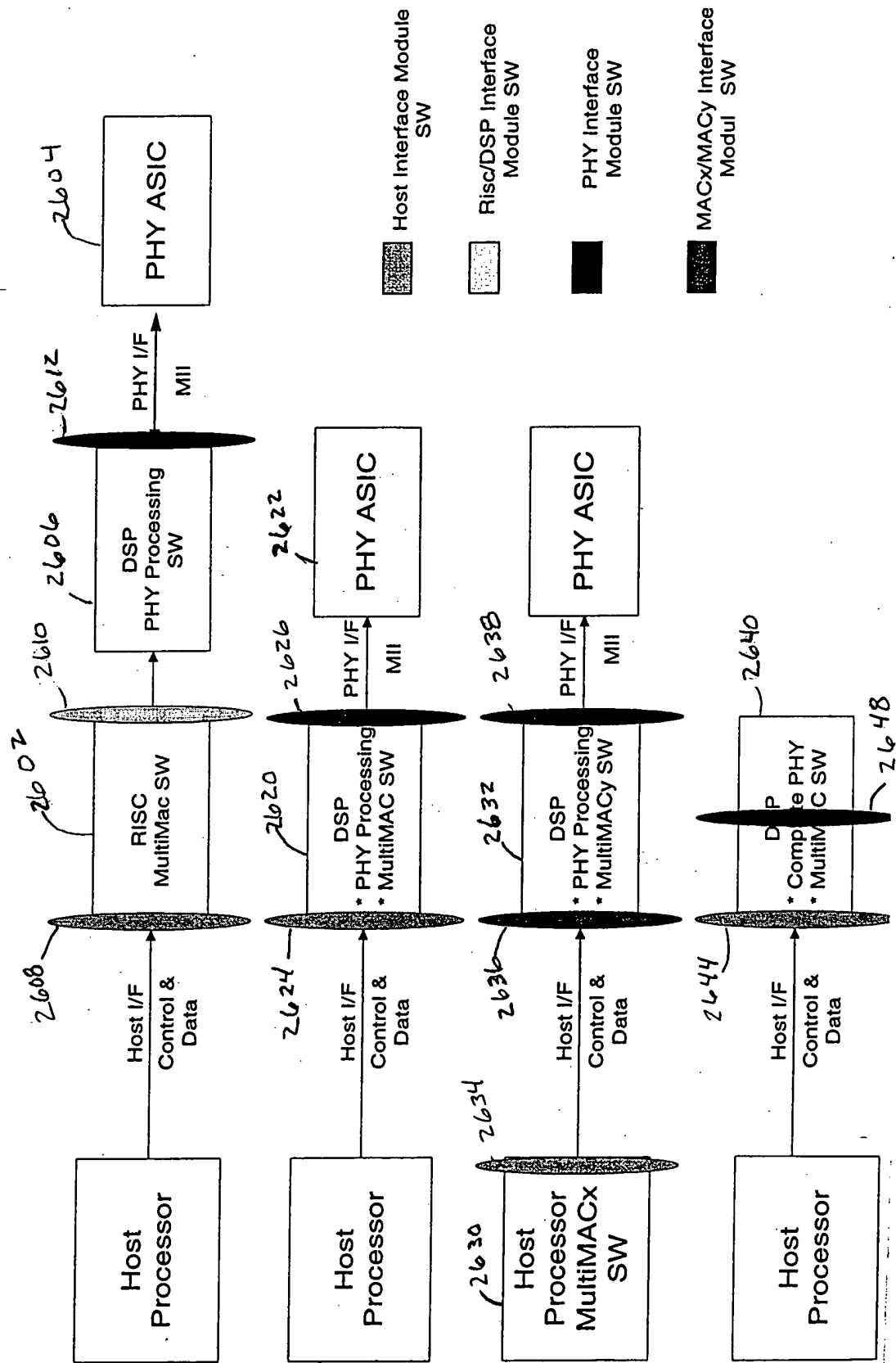


Figure 23

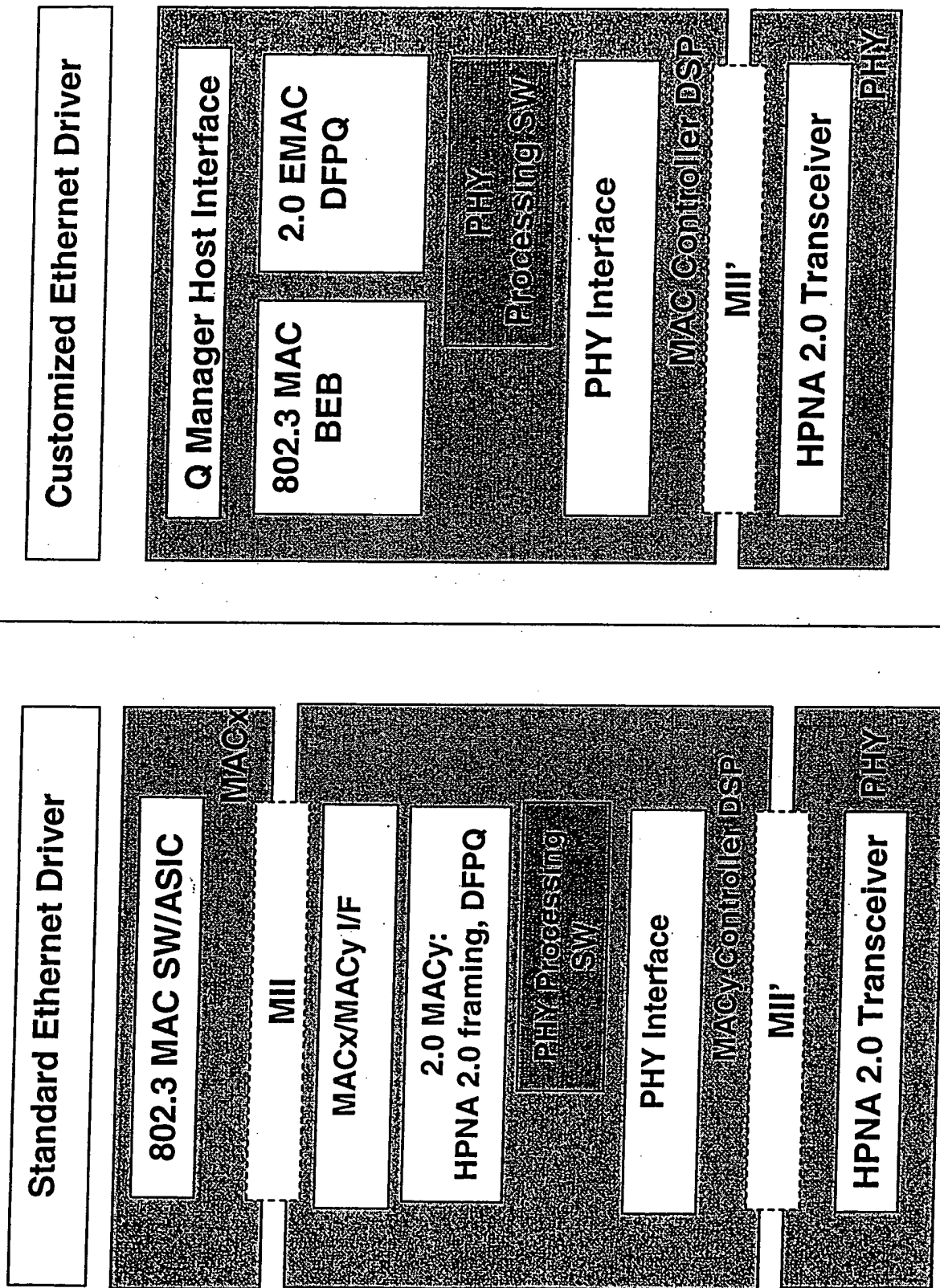


Figure 24